REMARKS

In an Office Action mailed on February 22, 2002, an objection was made to the drawings; an objection was made to the Abstract; claim 14 was rejected under 35 U.S.C. § 112, second paragraph; claims 1-3, 5, 6, 8, 9, 11, 12, 15, 16 and 18 were rejected under 35 U.S.C. § 102(e) as being anticipated by Nakajima; and claims 4, 7, 10, 13, 14 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakajima in view of Kinoshita. Fig. 4 has been amended, in a Proposed Drawing Amendment to overcome the objection to the drawings; the Abstract has been replaced to overcome the objection to the Abstract; and claim 14 has been amended to overcome the § 112, second paragraph rejection of claim 14. The §§ 102 and 103 rejections of the claims are addressed below.

Rejections of Claims 1-5:

The method of claim 1 specifies that during a refresh operation, a digital indication of a predetermined voltage is converted to an analog voltage to update a charge on a capacitor.

In contrast, Nakajima neither teaches nor suggests the above-recited limitation. In this manner, although Nakajima discloses an operating unit 23a that has a register that provides data to a digital-to-analog conversion circuit 25 ("DAC circuit 25"), Nakajima neither teaches nor suggests that the DAC circuit 25 converts the digital indication from the output register circuit 24 into an analog voltage to update a charge on a capacitor during a refresh operation. Furthermore, Nakajima does not mention a refresh operation in connection with its disclosed circuitry.

Thus, claim 1 overcomes the § 102 rejection in view of Nakajima. Claims 2-5 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 6-10:

The method of claim 6 includes providing capacitors and memory buffers. Each capacitor is associated with a different pixel cell to maintain a terminal voltage of the associated pixel cell near a predetermined voltage. Each memory buffer is associated with a different one of the pixel cells and stores a digital indication of the associated predetermined voltage. During a refresh operation, the digital indications are converted into analog voltages to update charges on the capacitors.

In contrast, Nakajima neither teaches nor suggests converting digital indications into analog voltages to update charges on capacitors during a refresh operation. As discussed above in connection with claim 1, Nakajima does not even mention a refresh operation.

Thus, claim 6 overcomes the § 102 rejection in view of Nakajima. Claims 7-10 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 11-15:

The light modulator cell of claim 11 includes a pixel cell, a capacitor, and a digital-to-analog converter. The capacitor maintains a terminal voltage of the pixel cell near a predetermined voltage. The memory stores a digital indication of the predetermined voltage, and the digital-to-analog converter converts the digital indication into an analog voltage to update a charge on the capacitor during a refresh operation. In contrast, as discussed above, Nakajima neither teaches nor suggests a digital-to-analog converter to convert a digital indication into an analog voltage to update a charge on a capacitor during a refresh operation, as Nakajima does not ever mention a refresh operation in connection with its disclosed circuitry.

Thus, claim 11 overcomes the § 102 rejection. Claims 12-15 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 16-18:

The light modulator of claim 16 includes pixel cells, capacitors, memory buffers and digital-to-analog converters. Each capacitor is associated with a different pixel cell to maintain a terminal voltage of the associated pixel cell near a predetermined voltage. Each memory buffer is associated with a different one of the pixel cells and stores a digital indication of the associated predetermined voltage. The digital-to-analog converters convert the digital indications into analog voltages to update charges on the capacitors during a refresh operation. In contrast, as discussed above, Nakajima neither teaches nor suggests digital-to-analog converters to convert digital indications into analog voltages to update charges on capacitors during a refresh operation.

Thus, withdrawal of the § 102 rejection of claim 16 is requested. Claims 17 and 18 are patentable for at least the reason that these claims depend from an allowable claim.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 102, 103 and 112 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0312US).

Respectfully submitted,

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